DESIGN & IMPLEMENTATION OF EFFICIENT MULTIPLIER USING FIXED WIDTH RPR

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Abstract— A reliable low area efficient multiplier is designed in this paper by using algorithmic noise tolerant architecture. The ANT architecture can achieve the demand of low power, high precision and area efficiency. ANT architecture contains a main digital signal processing block along with an error correction block. In error correction block a replica of main DSP block with reduced operands named as RPR block is used for error detection. Here different multipliers are used in main DSP block to check which performs well in ANT Architecture. The multipliers used in this paper are Baugh Wooley multiplier, Wallace Tree multiplier, Row Bypassing multiplier and Bypassing multiplier (Row and Column Bypassing multiplier).

Key words: ANT Architecture, RPR.

I. Introduction

In VLSI lowering the power and area of systems is the main aim. To lower the power dissipation voltage over scaling is in the process because CMOS circuit power is directly proportional to the square of supply voltage. This voltage over scaling leads to the reduction of signal to noise ratio (SNR). In algorithmic noise tolerant architecture voltage over scaling can be used to reduce the power but signal to noise ratio is maintained because of error correction block. Previously full width RPR is used in error correction block but to reduce complexity full width RPR is replaced with fixed width RPR. Using the fixed width RPR computation error can be occurred. A compensation circuit must be added to the fixed width RPR to reduce the computation error. By taking the use of probability, statistics and partial product weight analysis, an approximate compensation vector is found.

II. ANT Architecture:

There are two blocks present in the ANT architecture. One is main digital signal processing block another one is error correction block. Error correction block contains a reduced precision replica block along with the circuitry which checks the error occurred because of voltage over scaling in main digital signal processing block. The ANT architecture is as shown in fig.1.

Here the output of main block is referred as ya[n], output of RPR block is referred as yr[n] and output of error correction block is noted as $\hat{Y}[n]$.

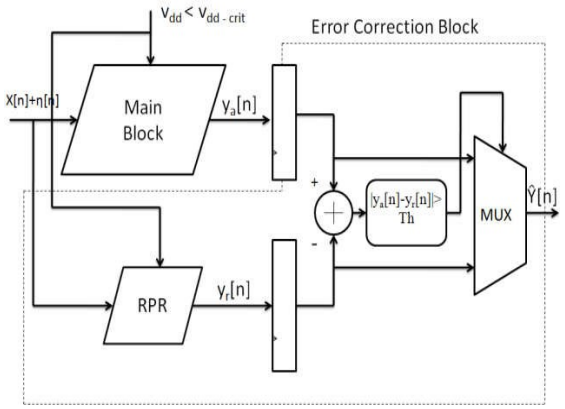

Fig1.ANT Architecture

RPR is a replica of main block with reduced

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precision operands and have shorter computation delay. Here fixed width RPR is taken instead of full width RPR to avoid infinite growth of bit width. If any soft errors occurred in main DSP block output ya[n], RPR output yr[n] is still correct since the critical path delay of replica is smaller than Tsamp. So yr[n] is used to detect errors in MDSP output by comparing the difference of |ya[n]-yr[n]| against a threshold value Th. If the difference between ya[n] and yr[n] is larger than the threshold value Th, the output Ŷ[n] is yr[n] else the output is ya[n]. So Ŷ[n] is expressed as

Ŷ[n]= ya[n], if |ya[n]-yr[n]| ≤Th
yr[n], if |ya[n]-yr[n]| >Th

The threshold value Th is determined as Th= max ∀input |y0[n]-yr[n]|

Where yo[n] is referred as error free output signal.

A full width (n/2) bit RPR can be divided into four subsets, which are most significant part (MSP), input correction vector (ICV), minor input correction vector (MICV) and least significant part (LSP). In the fixed width RPR only MSP part is kept and other parts are removed i.e. ICV, MICV, and LSP parts are truncated.

In the consideration of fixed width RPR a disadvantage is also present that there is a truncation error occurred because of the avoidance of ICV, MICV, LSB bits. To reduce the error, compensation circuit can be added to the fixed width RPR. The bits which are having highest weight in the truncated part are added as compensation circuit. Here ICV and MICV parts are used in compensation circuit because of their highest weighing.

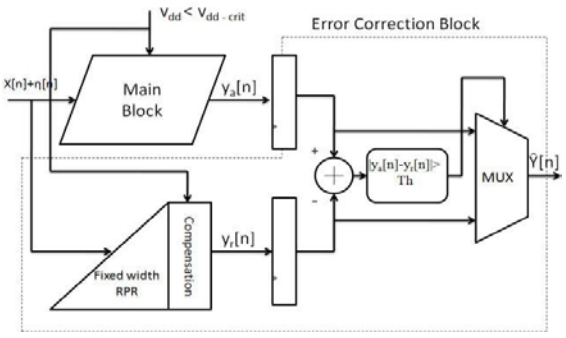


Fig 2: ANT Architecture with RPR compensation circuit

III. Baugh Wooley Multiplier

Baugh Wooley multiplier is used in the Main DSP block. Consider two unsigned inputs X and Y which are expressed as

$$X=\sum_{i=0}^{n-1} x_i 2^i \quad Y=\sum_{j=0}^{n-1} y_j 2^j$$

The result of multiplication can be expressed as

$$\sum_{k=0}^{2n-1} k_k 2^k = \sum_{i=0}^{n-1}\sum_{j=0}^{n-1} x_i y_j 2^{i+j} \quad (1)$$

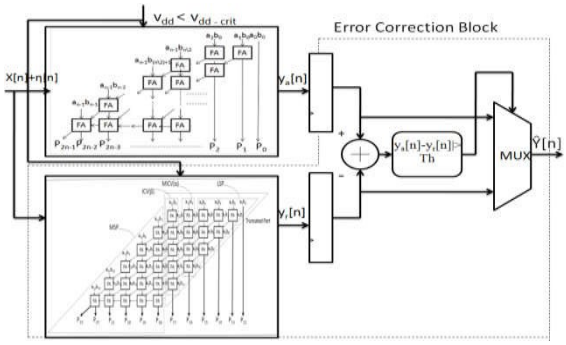


Fig 3: Baugh Wooley Multiplier in ANT architecture

For higher accuracy the error compensation circuit in the fixed width RPR can be set as shown in fig4.

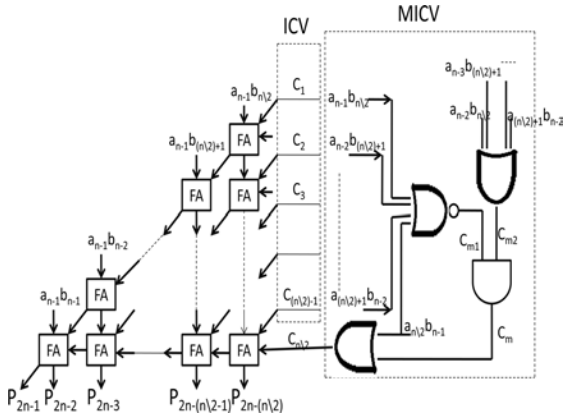


Fig 4: High accuracy fixed width RPR with compensation circuit constructed by ICV and MICV.

The output of fixed width multiplier Pt can be expressed as

$$P = \sum_{n-1}$$

$$X=\sum_{n-1} x\, 2i \quad Y=\sum_{n-1} y\, 2j$$

Where Error correction EC is expressed as f(EC)=f(ICV)+f(MICV)

IV. Row Bypass Multiplier

Generally a conventional full adder has three inputs and two outputs. When the operand bit of multiplier is zero the full adder has disadvantages such as low operational speed and unwanted switching activity. When zero partial products are added, a large number of signal transitions are generated and do not affect the final product. By using Row Bypassing multiplier zero partial products can be bypassed to achieve optimization. A modified full adder is used to achieve this optimization. The modified full adder is as in fig 5.

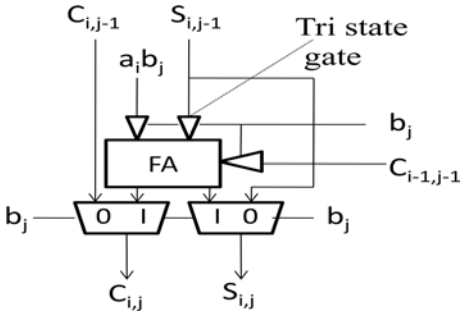
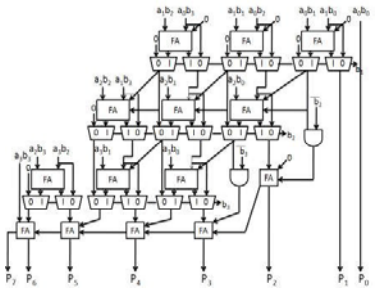


Fig 5: Structure of Full adder for Row Bypassing multiplier

In the design of n bit Row Bypass multiplier (n-1)x(n-1) full adders, 2x(n-1)x(n-1) multiplexers and 3x(n-1)x(n-1) three state gates are presented. A 4 bit Row Bypassing multiplier is as shown in fig 6.

A 12 bit Row Bypass multiplier can be designed and put in ANT architecture in the place of Baugh Wooley multiplier and performance was observed.

Fig 6: Row Bypass multiplier



V. Row and Column By passing Multiplier

Row and Column Bypassing multiplier is based on two dimensional bypassing features. According to this the addition operations in (i+1)th column or jth row can be bypassed if the bit in that corresponding column or row is zero. The addition operation in the (i+1,j)th adder can be bypassed if the product aibj is 0 and the carry bit ci,j-1 is 0. If the product bit aibj or the carry bit ci,j-1 is 1, the addition operation in that corresponding full adder will be executed. It reduces the power more than that of row bypassing multiplier. The circuitry used to build this multiplier is changed as shown in fig 7(a) and 7(b).

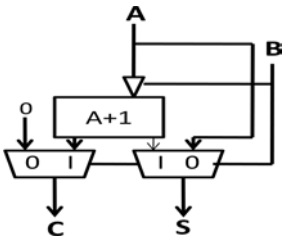


Fig 7(a): Half adder in Bypassing based design

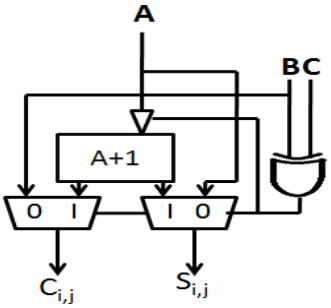


Fig 7(b): Full adder in Bypassing based design.

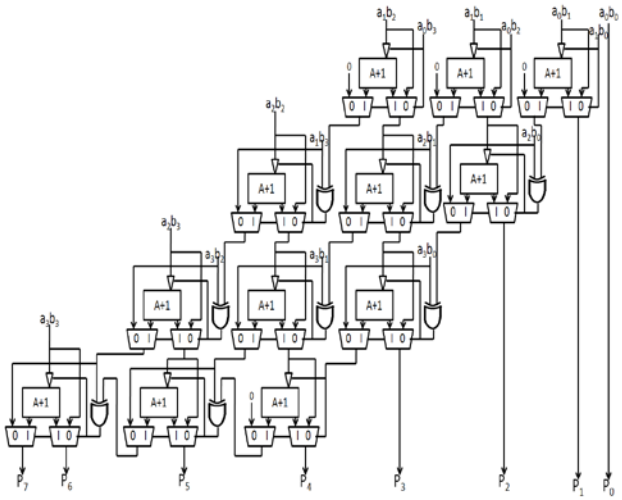


Fig 7(c): Row and Column Bypassing Multiplier

A 4 bit Row & Column bypassing multiplier is

as shown in fig 7(c). A 12 X 12 bit Row & Column Bypassing multiplier is replaced in place of Baugh Wooley multiplier in the ANT architecture to check its performance.

VI. Simulation Results

These are the simulation results of ANT architecture when 12 bit Baugh Wooley multiplier, 12 bit Row Bypass multiplier and 12 bit Row and Column Bypassing multiplier are used

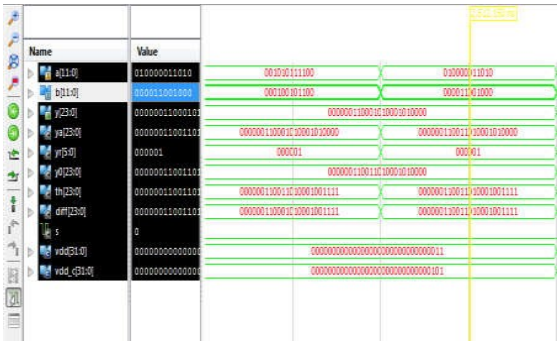


Fig 8: simulation result of ANT architecture when Baugh Wooley multiplier is used.

Fig 9: simulation result of ANT architecture when Row Bypassing multiplier is used.

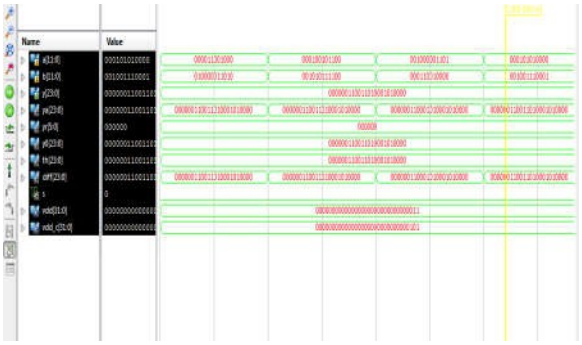


Fig 10: Simulation result of ANT architecture when Row and Column Bypassing multiplier is used.

VII. Conclusion

In the fixed width RPR based ANT design 12 bit Baugh Wooley multiplier, Row Bypassing multiplier and Row & Column bypassing multipliers are presented to check the area and delay performances.

The area and delay performance of Row & Column Bypassing multiplier is better than that of Baugh Wooley and Row Bypass multipliers.

The delay of Row & Column bypassing multiplieris 10% lower than Baugh Wooley multiplier and 7% less than that of Row Bypass multiplier. The area of Row & Column bypassing is 2% less than that of Baugh Wooley multiplier and 6% less than that of Row Bypass multiplier.

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